AMENDMENTS TO THE SPECIFICATION

Please replace the first full paragraph on page 15 of the specification with the following amended paragraph:

Fig. 2 is a block diagram showing a schematic arrangement of the tributary synchronization circuit 106. This tributary synchronization circuit 106 is constituted with frame bit detectors 202 that detects a position of a frame bit inserted in each of the tributary signals ~~114a~~ 113a to ~~114n~~ 113n, buffers 201 that stores the tributary signals, and a reference frame pulse generator 203 that generates a reference frame pulse 211 to be a timing for outputting tributary signals stored in the buffers 201.